WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

an SOI substrate including a first semiconductor region, a buried insulating film formed on the first semiconductor region, and a second semiconductor region formed on the buried insulating film;

a trench with a depth to reach the first semiconductor region, extending from a surface of the second semiconductor region in the SOI substrate and passing through the buried insulating film;

a trench capacitor formed within the trench; and

a conductive layer formed in a region between a sidewall portion of the trench and the buried insulating film, the conductive layer electrically connecting the first semiconductor region and the second semiconductor region.

2. A semiconductor device according to claim 1, further comprising a transistor formed in the second semiconductor region in the SOI substrate and forming a logic circuit.

3. A semiconductor device according to claim 2, further comprising a silicide layer provided on at least a part of a gate electrode, a source region and a drain region of the transistor forming the logic circuit.

4. A semiconductor device according to claim 1, further comprising a transistor formed in the second

semiconductor region in the SOI substrate, one of a source region and a drain region of the transistor being connected to one electrode of the trench capacitor, the transistor and the trench capacitor forming a DRAM memory cell.

5. A semiconductor device according to claim 4, further comprising a transistor formed in the second semiconductor region in the SOI substrate and forming a logic circuit.

6. A semiconductor device according to claim 5, further comprising a silicide layer provided on at least a part of a gate electrode, a source region and a drain region of the transistor forming the logic circuit.

7. A method of manufacturing a semiconductor device, comprising:

forming a trench in an SOI substrate, the trench extending from a major surface of the SOI substrate and passing through a buried insulating film;

forming a first insulating film in the trench, the first insulating film with a depth to reach an upper surface of the buried insulating film;

forming a second insulating film in a sidewall portion of the trench above the first insulating film, the second insulating film made of a material different from that of the first insulating film;

etching back the first insulating film to such

a depth as to reach an upper surface of the buried insulating film, using the second insulating film as a mask, and recessing the buried insulating film exposed to the sidewall portion of the trench;

forming a semiconductor layer by epitaxial growth in a gap created by the recessed buried insulating film; and

removing the first insulating film and the second insulating film and forming a trench capacitor in the trench.

8. A method according to claim 7, further comprising forming a first transistor in the SOI substrate, wherein the first transistor and the trench capacitor form a DRAM memory cell.

9. A method according to claim 7, further comprising forming a second transistor in the SOI substrate, wherein the second transistor forms a logic circuit.

10. A method according to claim 8, further comprising forming a second transistor in the SOI substrate, wherein the second transistor forms a logic circuit.

11. A method according to claim 10, wherein at least a part of a manufacturing process of the transistor forming the DRAM memory cell is common to that of the transistor forming the logic circuit.

12. A method according to claim 7, wherein the SOI

substrate is formed by bonding oxide film sides of two semiconductor substrates each having the oxide film on one surface thereof.

13. A method of manufacturing a semiconductor device, comprising:

forming a trench in an SOI substrate, the trench extending from a major surface of the SOI substrate and passing through a buried insulating film;

forming a first insulating film in the trench, the first insulating film with a depth to reach an upper surface of the buried insulating film;

forming a second insulating film in a sidewall portion of the trench above the first insulating film, the second insulating film made of a material different from that of the first insulating film;

etching back the first insulating film to such a depth as to reach an upper surface of the buried insulating film, using the second insulating film as a mask, and recessing the buried insulating film exposed to the sidewall portion of the trench;

depositing a polysilicon layer on a major surface of the SOI substrate and in the trench;

etching back the polysilicon layer by performing anisotropy etching to cause the polysilicon layer to remain in a gap created by the recessed buried insulating film in the trench; and

removing the first insulating film and the second

insulating film and forming a trench capacitor in the trench.

14. A method according to claim 13, further comprising forming a first transistor in the SOI substrate, wherein the first transistor and the trench capacitor form a DRAM memory cell.

15. A method according to claim 13, further comprising forming a second transistor in the SOI substrate, wherein the second transistor forms a logic circuit.

16. A method according to claim 14, further comprising forming a second transistor in the SOI substrate, wherein the second transistor forms a logic circuit.

17. A method according to claim 16, wherein at least a part of a manufacturing process of the transistor forming the DRAM memory cell is common to that of the transistor forming the logic circuit.

18. A method according to claim 13, wherein the SOI substrate is formed by bonding oxide film sides of two semiconductor substrates each having the oxide film on one surface thereof.